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TRANSFORMERLESS RESONANT CONVERTER BASED FOR AC MODULE APPLICATION

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Abstract: **The proposed design features high efficiency over a wide input and output voltage range, step up voltage conversion, small size, and excellent transient performance. This aim of the project to improve the efficiency by using a scheme based on continuous conduction mode (CCM).Resonant DC-link inverter technique becomes dominate in solving the problems due to its simplicity in both power stage topology and control strategy. In addition, a resonant gate drive scheme is presented which provides rapid start up and low-loss at HF and VHF frequencies. The converter regulates the output using an on-off control scheme modulating at a fixed frequency. This control method enables fast transient response and efficient light load operation while providing controlled spectral characteristics of the input and output waveforms. The stability of the resonant converter in CCM has been verified at selected working conditions. The proposed single-stage inverter not only provides HPF to the utility line, but also achieves circuit simplicity, low cost, and high reliability.**

I. INTRODUCTION

Motor drives rely on semiconductor power devices for power conditioning. The emergence of mature power devices, such as SCR, GTO and IGBT, makes it possible to handle power processing up to IMW. However the conventional PWM voltage source inverter (VSI) can not fully take the advantages of these advances in power semiconductor. Typically, VSI drive is suitable for dc/ac inverter applications in the power range of lOW-500kW[I]. This is mainly due to the following reasons:

a) high switching losses at higher switching frequency;
b) high dv/dt spikes;
c) large SOA specifications required;
d) high acoustic noise;
e) poor ac line harmonics.

As has long been recognized, a substantial increase in inverter switching frequency is required to be able to rrumrmze low order harmonics in PWM-type applications. High switching frequencies have the concomitant advantages of higher current regulator bandwidth, smaller reactive component size, and for frequencies above 18kHz, acoustic noise which is above the threshold of human perception[2]. Basically, increasing switching frequency of motor drive has been accomplished following two approaches. By improving device speed and SOA ratings, from 500Hz to 2kHz, motor drives rated 1-25kW can be achieved[l]. The other approach to boost the switching frequency is based on improving the switching environment to maximize device utilization[I-5]. Using snubber circuit to reduce the switching losses and relieve high stresses is one of most common methods. The principle of using snubber circuit to improve switching environment is modification of switching loci for a bipolar junction transistor (BJT). Unfortunately, the introduction of snubber circuit results in increased complexity of the drive circuit. Consequently, the increase in frequency is obtained with the heavy penalty 111 terms of high cost and low system efficiency.

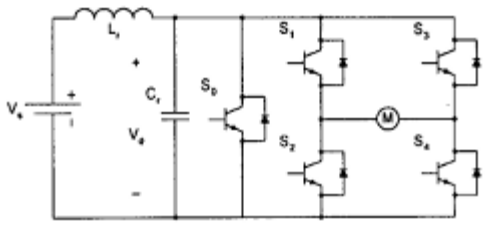

Fig. 1 Resonant DC-link inverter

Recent literature shows a new trend of incorporating resonant technique into conventional VSI topology. By introducing a resonant link

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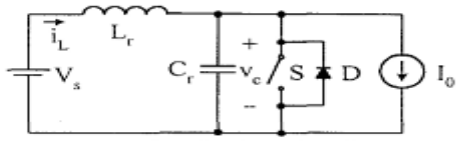
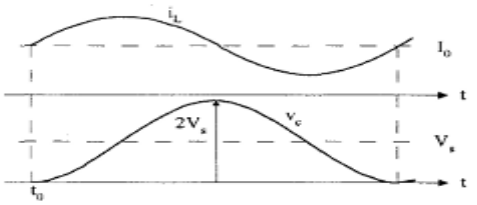
between the source and the switch network, zero- switching environment is created. Switching losses in these circuits are remarkably reduced. As a result, operation at high frequency up to 50kHz is possible to be achieved. In 1989, a resonant de-link inverter topology was proposed by D. M. Divan] l], as shown in Fig. I. This circuit is attractive due to its simplicity in both power stage and control circuit. The principle of operation of the resonant de-link inverter will be described in the following section

II. PRINCIPLE OF OPERATION OF THE DC-LINK INVERTER

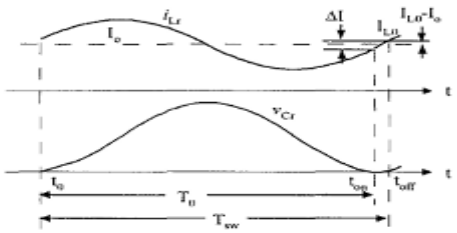
The operation of the resonant de link inverter can be found in [1,2,6,7]. A simplified circuit is illustrated in Fig. 2(a), in which 10 represents the instantaneous current being supplied by the inverter to the motor.



(a) Equivalent circuit



(b) Waveforms under lossless condition



(c) Waveforms under loss condition

Fig. 2 Resonant dc-link inverter

Fig. 2 Resonant de-link inverter. Firstly, let's consider loss less case. Initially, the capacitor voltage *vc,.(to)* is zero and *iLrCto)* is 1o. **It** is easy to find that the capacitor voltage

$$vcr(t)=V,Jl\text{-}coscoo(t\text{-}to)], \quad (1)$$

Where,

wo = 1 / Lr/Cr,At wo (t-t0)=Vcr(t) (2) returns to zero and *iLr(t)* returns to 10, thus setting up the desired switching condition for the switches in the inversion bridges. In this lossless case, S can be removed. Fig. 2(b) shows the resonant voltage and current waveforms of such an idealized circuit.

When conduction losses are considered, *irr(t)* and *ver(t)* will no longer be able to return to 10 and zero, respectively, at the end of each resonant cycle because of the damping effect. Thus the ZVS switching condition is lost. In order to compensate for the energy loss in each resonant cycle, a short interval is introduced by turning on and off S before the beginning of each resonant cycle so that the inductor current lLO is greater than 1o. The waveforms under such operation are shown in Fig. 2(c).

Assuming that the system is highly under-damped, *vCr(t)* can be expressed approximately as:

$$vCr\,(t) = Vdc + e\text{-}R(1\text{-}Io)/2L,$$

$$. [COoLr(lLo\ \text{-}1()\sin\ COo(t\text{-}\ to)\ \text{-}\ Vdc\cos COo(t\text{-}\ to)] \quad (3)$$

It can be seen that the capacitor voltage depends on the difference between lLO and 1o. If the time period introduced is too long and lLO is much larger than 1o, then *vcrCt)* will have a peak value significantly larger than 2Vs. Therefore, the interval during which S remains on must be controlled to ensure that ho-Io does not exceed the desired value. Because of this interval, the power switch is now driven on and off at a frequency **z,** a little bit smaller than the resonant frequency of the Lr, C, resonant tank.

Finally, it is interesting to note that in Fig. 2(a), switch S is in parallel with two switches comprising an inverter leg and hence it can also be removed, resulting in a more simplified inverter topology for the proposed ac drive application.

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III. DESIGN OF 200HP MOTOR DRIVE

A. Control strategy

The primary objective of this work is to design a single phase high power (up to 200HP) motor drive. A load current command (with a certain phase advance) is given by a sinusoidal signal generator. Figure 3 shows one of the drive strategies for the resonant de-link inverter shown in Fig. I. In this strategy, the load current iM(t) is compared with the current command icmd(t). By sampling the compared result at the end of each switching cycle, the control circuit determines the conduction mode of the four switches in next switching cycle. The control rule is:

$$\mathrm{Sign}[i_{cmd}(t_k)]\cdot\mathrm{Sign}[\,|i_{cmd}(t_k)| - |i_M(t_k)|\,]$$

$$= \begin{cases} +1 \text{ — } S_1, S_4 \text{ ON; } S_2, S_3 \text{ OFF} \\ -1 \text{ — } S_2, S_3 \text{ ON; } S_1, S_4 \text{ OFF} \end{cases}$$

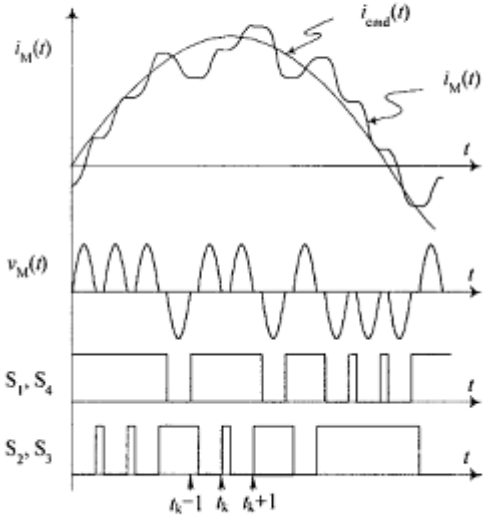

Fig. 3 Control strategy for resonant dc-link inverter

In the beginning of each switching cycle, let's have a short interval *i\t,* during which, all the four switches will be turned on so that the resonant tank can get energy compensation as mentioned in Section II.

B. Design procedure

Constraint 1: Set the linear increment of resonant inductor current i\I for energy compensation in each switching cycle (shown in Fig. 2(c» as

$$M = 1" \text{ xlO\%} \quad (4)$$

Constraint 2: The peak resonant inductor current

$$I_{Lr}\ pk = 6kA. \quad (5)$$

Constraint 3: The peak resonant capacitor voltage

$$Vcr,pk = lkV. \quad (6)$$

Constraint 4: Resonant inductance is much smaller than the load inductance:

$$Lr \ll L. \quad (7)$$

Based on the four constraints, a 200HP resonant de-link inverter is designed as follow.

Specifications:

Load (motor parameters):

L= 11.48IJ.H;

R= 0.624mn;

Vemf= 134.3V (rms)

Switching frequency.j.; = 50kHz (Tsw = 20lJ.s)

Output fundamental frequencyrj[= 1.632kHz

Output current: 10 = 1170.6A (rms)

Phase advance: ¢ = 30°

Input voltage: Vdc= 350 V_{DC}

Design.:

By neglecting the exponential attenuation 111 Eq.(3) we have

$$VCr(I) = V'/C + [Z, (ILo \pm iM(I))\sin 0V - Vdc\cos 0V] \quad (8)$$

$$i"(t) = iM(t) + [\sim: \sin roo' + (1, _0 \pm iM(I))\cos roo' \quad (9)$$

Where

Zo=root of Lr/cr (10)

Basically, the task of design for a resonant circuit is to determine the value of resonant inductance L, and resonant capacitance C"

In Eqs.(8) and (9), the "+" sign is applied

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when

$$\begin{cases} I^{-}_{Lr,pk} \approx I_{o,pk} + \dfrac{V_{dc}}{Z_o} \\ I^{+}_{Lr,pk} = I_{o,pk} + \sqrt{\left(\dfrac{V_{dc}}{Z_o}\right)^2 + \left(2.1 I_{o,pk}\right)^2} \end{cases} \quad (12)$$

Where,

$V^{-}_{Cr,pk}$ — peak resonant capacitor voltage when conduction path of the switch network has not been changed;

$I^{-}_{Lr,pk}$ — peak resonant inductor current when conduction path of the switch network has not been changed;

$V^{+}_{Cr,pk}$ — peak resonant capacitor voltage when conduction path of the switch network has been changed;

$I^{+}_{Lr,pk}$ — peak resonant inductor current when conduction path of the switch network has been changed;

$I_{o,pk}$ — peak output current

($I_{o,pk} = 1170.6 \times \sqrt{2} = 1.65kA$).

In order to satisfy **Constrain 2**, $I^{+}_{Lr,pk} = 6kA$, let's solve Eq.(12) for Z_o,

$$Z_o = \frac{V_{dc}}{\sqrt{\left(I^{+}_{Lr,pk} - I_{o,pk}\right)^2 - \left(2.1 I_{o,pk}\right)^2}} \quad (13)$$

$$\approx \frac{350V}{2645.8A} \approx 0.132\,\Omega$$

= 923.0V.

= 923.0V.

$$\frac{L_r}{L} = \frac{0.42\mu H}{11.48\mu H} << 1.$$

Therefore, the designed L_r and C_r satisfy all the four constraints. The voltage and current stresses on the switches are:

For S_1~S_4 and D_1~D_4:

Current stress: 1.65kA

Voltage stress: 923V.

IV. CONTROL CIRCUIT AND SIMULATION PARAMETERS

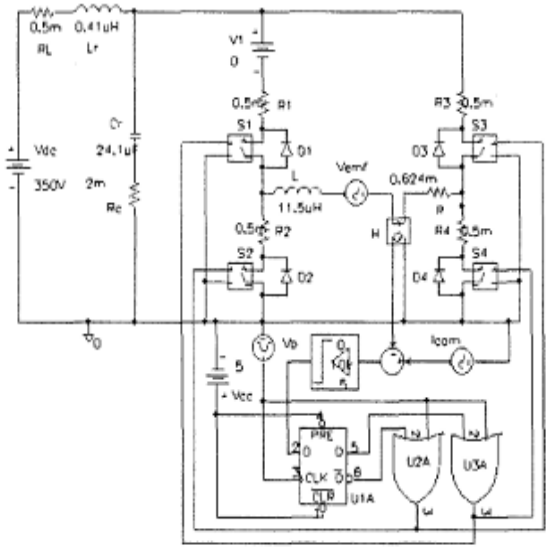

Fig. 4 Simulation schematic for the designed

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On the other hand, during the linear charging period of resonant inductor, we have

$$M = \underset{LeI'}{V_{dc}} !1t = \underset{()}{I} \text{ x } 10\% = 117A \quad (14)$$

and,

$$tJ.f=T,w \; -t; =20)J.S-2n\sim LrCr \quad (15)$$

Solving Eq.(13)-(1S) and considering , we obtain the following design results:

L, = 0.42IlH; C_r = *24.0IlF;* tJ.t= *0.5Ils.*

Now, let's check Constrain 3, *Vcr,pk<lkV,* and Constrain 4, Lr«L:

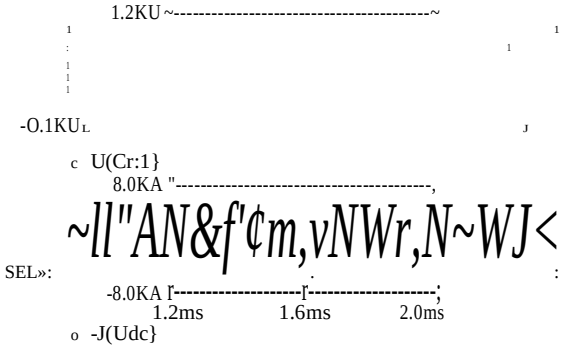
$$VCr_{pk} = V(:._{pk} = V_{dc} + \sim(2.1 \text{ x } lo_{pk} \; Z0)2 + r:$$

$$=350+ \quad (2.IXI650X \quad \sim 0.42)2 \quad +3502$$

24.S

resonant de-link inverter

Fig. 4 shows the schematic of the designed resonant de-link inverter together with its control circuit for the PSPICE simulation. The 200HP motor is modeled by a serial branch formed by L, R and back EMF V emf. leom is a sinusoidal current command, which has 30° phase difference leading the back EMF voltage. The load current is sensed by a transducer modeled by H with a certain transform ratio. The output of H is compared with the current command to generate a signal for the D- flip-flop UIA and determine which of the switches SI and S4 or Switches S2 and S3 must be turned on. The pulse voltage source vp serves as synchronizing signal (with switching frequency) and its pulse width provides a short interval to turn on all the switches for energy compensation as mentioned in Section II.



Time

Fig. 5 Simulated capacitor voltage (upper) and input current (lower)

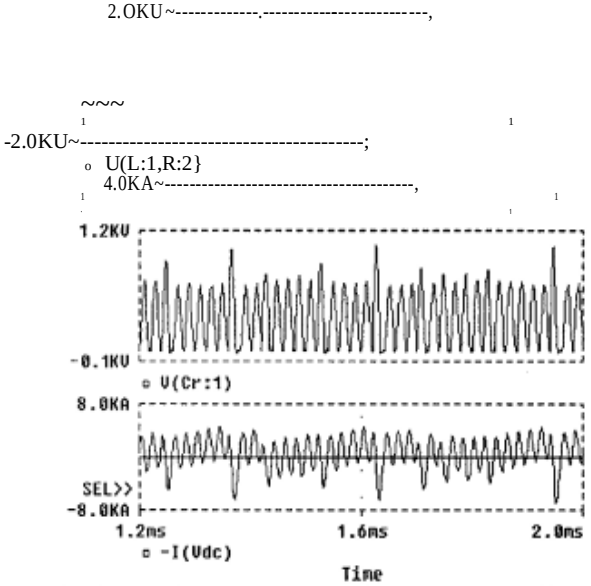


Fig. 5 Simulated capacitor voltage (upper) and input current (lower)

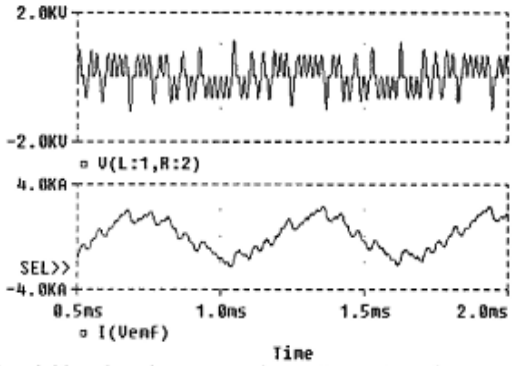


Fig. 6 Simulated motor voltage (upper) and current (lower)

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Figure 7 shows the frequency spectra of the motor voltage and current waveforms. **It** can be seen that the harmonic components mainly exist in the low frequency range, implying less EMI.

VII. CONCLUSIONS

Resonant DC-link inverter is able to provide effective treatments for high EMI, acoustic noise, poor harmonic contents and low frequency operation problems. Both analysis and PSPICE simulation results show that at high frequency operation, the resonant DC-link inverter gives limited frequency range of harmonics, which ensures low EMI. The inverter efficiency is also significantly higher than its hard switching counterpart, implying the capability of high frequency operation. In the design of resonant DC- link inverter for high power applications, voltage and current stresses of switches are crucial. In selecting the switching devices, satisfying these stresses should be set as design constraints.

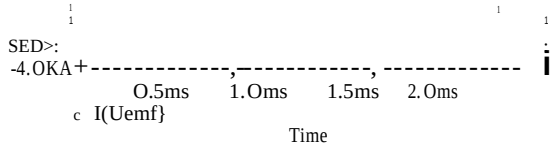

Fig. 6 Simulated motor voltage (upper) and current (lower)

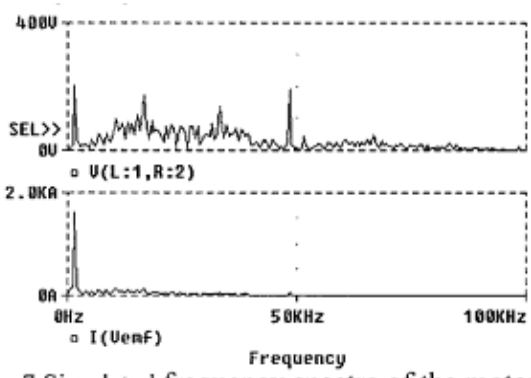

Fig. 7 Simulated frequency spectra of the motor voltage (upper) and current (lower)

The simulation results for the resonant de-link inverter are given in Figs. 5, 6 and 7. **It** is clearly shown in Fig. 5 that the motor voltage and the capacitor voltage are trains of resonant pulses that start and end at about zero volt. Thus it ensures the soft-switching for the switches. We also noticed that the maximum resonant capacitor voltage is about lkV and the maximum supply current is about 7kA, which are close to the design specifications ($V_{peak:}$ lkV, $I_{peak:}$ 6kA).

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